CLAIMS

1. A non-volatile memory device comprising:

a semiconductor substrate;

a source region and a drain region formed in the substrate;

an impurity region formed between the source region and the drain region, wherein the impurity region is in a floating state;

a vertical structure located between the source region and the impurity region on a first area of the semiconductor substrate such that a tunneling layer, a charge trapping layer, and a blocking layer are sequentially stacked between the source region and the impurity region;

a control gate insulating layer located between the source region and the impurity region, the control gate insulating layer adjacent to the vertical structure;

a control gate electrode that is formed on the vertical structure and the control gate insulating layer;

a gate insulating layer located between the impurity region and the drain region on the semiconductor substrate; and

a gate electrode on the gate insulating layer.

2. The non-volatile memory device of claim 1, wherein the charge trapping layer is nonconductive.

3. The non-volatile memory device of claim 1, wherein the first area in which the vertical structure is formed is adjacent to the source region.

4. The non-volatile memory device of claim 1, further comprising a metal silicide layer that is formed on the control gate electrode.

5. The non-volatile memory device of claim 1, wherein the control gate insulating layer is thinner than the vertical structure.

6. The non-volatile memory device of claim 1, further comprising an insulating layer spacer located at a sidewall towards the impurity region among sidewalls of the vertical structure and the control gate electrode.

7. The non-volatile memory device of claim 6, wherein the gate electrode has a sidewall gate structure on the insulating layer spacer.

8. A non-volatile memory device comprising:

a semiconductor substrate;

a source region and a drain region;

a first impurity region and a second impurity region between the source region and the drain region, the first impurity region being in a floating state and adjacent to the source region and the second impurity region being in the floating state and adjacent to the drain region;

a first vertical structure between the first impurity region and the second impurity region and adjacent to the first impurity region, the first vertical structure including a first tunnelling layer, a first charge trapping layer, and a first blocking layer that are sequentially stacked;

a second vertical structure between the first impurity region and the second impurity region and adjacent to the second impurity region, the first vertical structure including a second tunnelling layer, a second charge trapping layer, and a second blocking layer that are sequentially stacked;

a control gate insulating layer between the first vertical structure and the second vertical structure;

a control gate electrode on the first vertical structure, the control gate insulating layer, and the second vertical structure;

a first gate insulating layer between the source region and the first impurity region;

a first gate electrode on the first gate insulating layer;

a second gate insulating layer between the second impurity region and the drain region; and

a second gate electrode on the second gate insulating layer.

9. The non-volatile memory device of claim 8, wherein the first charge trapping layer and the second charge trapping layer are nonconductive.

10. The non-volatile memory device of claim 8, further comprising a metal silicide layer on the control gate electrode.

11. The non-volatile memory device of claim 8, wherein the control gate insulating layer is thinner than the first vertical structure and the second vertical structure.

12. The non-volatile memory device of claim 8, further comprising a first insulating layer spacer at a sidewall toward the first impurity region among sidewalls of the first vertical structure and the control gate electrode.

13. The non-volatile memory method of claim 12, wherein the first gate electrode has a sidewall gate structure on the first insulating layer spacer.

14. The non-volatile memory device of claim 8, further comprising a second insulating layer spacer at a sidewall toward the second impurity region among sidewalls of the second vertical structure and the control gate electrode.

15. The non-volatile memory device of claim 14, wherein the second gate electrode has a sidewall gate structure on the second insulating layer spacer.

16. A method for fabricating a non-volatile memory device, the method comprising:

sequentially forming a first insulating layer for forming a tunnelling layer, a nonconductive substance layer for forming a charge trapping layer, and a second insulating layer for forming a blocking layer on a semiconductor substrate;

forming a first mask layer pattern on the second insulating layer;

etching the tunnelling layer, the charge trapping layer, and the blocking layer using the first mask layer pattern as an etching mask, to form a vertical structure;

removing the first mask layer pattern after the etching process is completed;

forming an oxide layer for forming a control gate insulating layer and a gate insulating layer of a select transistor on the semiconductor substrate exposed by the vertical structure;

forming a conductive layer for forming a control gate electrode and a gate electrode of the select transistor on the oxide layer and the vertical structure;

forming a second mask layer pattern on the conductive layer;

defining the control gate electrode on the vertical structure and the control gate insulating layer on a first region of the semiconductor substrate by performing an etching process using the second mask layer pattern as an etching mask and defining the gate electrode on the gate insulating layer on a second region of the semiconductor substrate;

removing the second mask layer pattern; and

forming a source region, an impurity region, and a drain region that are aligned with the control gate electrode and the gate electrode by performing an impurity ion implantation process.

17. The method of claim 16, wherein the first insulating layer is formed of silicon oxide by thermal oxidation, the nonconductive substance layer is formed of nitride by chemical vapor deposition, and the second insulating layer is formed of oxide by chemical vapor deposition.

18. The method of claim 16, wherein the method further comprises forming a metal silicide layer on the conductive layer.

19. A method for fabricating a non-volatile memory device, the method comprising:

sequentially forming a first insulating layer for forming a tunnelling layer, a nonconductive substance layer for forming a charge trapping layer, and a second insulating layer for forming a blocking layer on a semiconductor substrate;

forming a first mask layer pattern on the second insulating layer;

forming a vertical structure with the tunnelling layer, the charge trapping layer, and the blocking layer by performing an etching process using the first mask layer pattern as an etching mask;

removing the first mask layer pattern after the etching process is completed;

forming a third insulating layer for forming a control gate insulating layer on the semiconductor substrate exposed by the vertical structure;

forming a first conductive layer for forming a control gate electrode on the third insulating layer and the vertical structure;

forming a second mask layer pattern on the conductive layer for forming the control gate electrode;

defining the control gate electrode on the vertical structure and the control gate insulating layer on a first region of the semiconductor substrate by performing the etching process using the second mask layer pattern as the etching mask;

removing the second mask layer pattern;

forming an impurity region on a certain area of the semiconductor substrate by performing an ion implantation process using the control gate electrode and a predetermined first ion implantation mask layer as a mask;

forming a fourth insulating layer that forms an insulating layer spacer covering the control gate electrode and the semiconductor substrate and forms a gate insulating layer of a select transistor;

forming a second conductive layer for forming a gate electrode of the select transistor on the fourth insulating layer;

forming an insulating layer spacer at a sidewall of the control gate electrode that is opposite to the vertical structure by performing an anisotropic etching process on the second conductive layer and the fourth insulating layer;

forming a gate electrode in the form of a sidewall gate on the insulating layer spacer; and

forming a source region and a drain region on by implanting impurity ions into the semiconductor substrate exposed by the control gate electrode and the gate electrode.

20. The method of claim 19, wherein the first insulating layer is formed of silicon oxide by thermal oxidation, the nonconductive substance layer is formed of nitride by chemical vapor deposition, and the second insulating layer is formed of oxide by chemical vapor deposition.

21. The method of claim 19, wherein the method further comprises forming a metal silicide layer on the first conductive layer.

22. The method of claim 19, wherein the anisotropic etching process performed on the second conductive layer and the fourth insulating layer is performed using an etching back process.

23. A method for fabricating a non-volatile memory device, the method comprising:

sequentially forming a first insulating layer for forming a first and a second tunnelling layer, a nonconductive substance layer for forming a first and a second charge trapping layer, and a second insulating layer for forming a first and a second blocking layer on a semiconductor substrate;

forming a first mask layer pattern on the second insulating layer, the first mask layer pattern covering a first region and a second region of the semiconductor substrate;

forming on the first region a first vertical structure comprising the first tunnelling layer, the first charge trapping layer, and the first blocking layer by performing an etching process using the first mask layer pattern as an etching mask;

forming on the second region a second vertical structure comprising the second tunnelling layer, the second charge trapping layer, and the second blocking layer by performing the etching process using the first mask layer pattern as the etching mask;

removing the first mask layer pattern after the etching process is completed;

forming a third insulating layer for forming a control gate insulating layer, a first gate insulating layer of a first select transistor, and a second gate insulating layer of a second select transistor on the semiconductor substrate exposed by the first vertical structure and the second vertical structure;

forming a conductive layer for forming a control gate electrode, a first gate electrode of the first select transistor, and a second gate electrode of the second transistor on the third insulating layer, the first vertical structure, and the second vertical structure;

forming a second mask layer pattern on the conductive layer;

defining the control gate electrode aligned with the first vertical structure and the second vertical structure, defining the first gate insulating layer and the first gate electrode on the semiconductor substrate that is separated from a sidewall of the control gate electrode, and defining a second gate insulating layer and a second gate electrode on the semiconductor substrate which is separated from the other sidewall of the control gate electrode, by performing an etching process using the second mask layer pattern as the etching mask;

removing the second mask layer pattern; and

forming a source region, a first impurity region, a second impurity region, and a drain region on the semiconductor substrate so as to be aligned with the control gate electrode, the first gate electrode and the second gate electrode, by performing an ion implantation process.

24. A method for fabricating a non-volatile memory device, the method comprising:

sequentially forming a first insulating layer for forming a tunnelling layer, a nonconductive substance layer for forming a charge trapping layer, and a second insulating layer for forming a blocking layer on a semiconductor substrate;

forming a first mask layer pattern on the second insulating layer, the first mask layer pattern covering a first region and a second region of the semiconductor substrate;

forming a first vertical structure where a first tunnelling layer, a first charge trapping layer and a first blocking layer are sequentially stacked on the first region, and forming a second vertical structure where a second tunnelling layer, a second charge trapping layer and a second blocking layer are sequentially stacked on the second region, by performing an etching process using the first mask layer pattern as an etching mask;

removing the first mask layer pattern after the etching process is completed;

forming a third insulating layer for forming a control gate insulating layer, a first gate insulating layer of a first select transistor, and a second gate insulating layer of a second select transistor on the semiconductor substrate exposed by the first vertical structure and the second vertical structure;

forming a first conductive layer for forming a control gate electrode on the third insulating layer, the first vertical structure, and the second vertical structure;

forming a second mask layer pattern on the first conductive layer;

defining the control gate electrode on the first vertical structure, the second vertical structure, and the control gate insulating layer on a first region of the semiconductor substrate by performing an etching process using the second mask layer pattern as the etching mask;

removing the second mask layer pattern;

forming a first impurity region and a second impurity region at both sidewalls of the control gate electrode by performing an ion implantation process using the control gate electrode and a predetermined ion implantation mask layer as a mask;

forming a fourth insulating layer for forming a first gate insulating layer of a first select transistor and a second gate insulating layer of a second select transistor so as to cover the control gate electrode and an exposed portion of the semiconductor substrate;

forming a second conductive layer for forming a first gate electrode of the first select transistor and a second gate electrode of the second select transistor on the fourth insulating layer;

forming a first insulating spacer and a second insulating spacer at both sidewalls of the control gate electrode by performing an anisotropic etching process on the second conductive layer and the fourth insulating layer, and forming a first gate electrode and a

second gate electrode in the form of sidewall gates on the first insulating spacer and the second insulating spacer, respectively; and

forming a source region and a drain region by implanting impurity ions into the semiconductor substrate exposed by the control gate electrode, the first gate electrode, and the second gate electrode.

25. The method of claim 24, wherein the anisotropic etching process comprises an etching back process.

26. A method for fabricating a non-volatile memory device, the method comprising:

forming a source region, a drain region, and an impurity region on a semiconductor substrate, the impurity region between the source region and drain region and configured to be maintained in a floating state;

sequentially stacking a tunneling layer, a charge trapping layer, and a blocking layer between the source region and the impurity region, thereby forming a vertical structure;

forming a control gate insulating layer adjacent to the vertical structure and between the source region and the drain region;

forming a control gate electrode on the vertical structure and the control gate insulating layer;

forming a gate insulating layer between the impurity region and the source region; and

forming a gate electrode on the gate insulating layer.

27. The method of claim 26, wherein the vertical structure comprises an oxide-nitride-oxide structure.